THE CLAIMS

1. (Previously Presented) An apparatus for display of video data from a plurality of video sources, the apparatus comprising:

a plurality of video decoders configured to be coupled to different video sources, each video decoder comprising:

an output, and

an input configured to be coupled to a video source, to receive video data from the video source, and to decode the received video data;

a switch network including an output and an input coupled to the video decoder outputs; and

a plurality of video processing pipelines, each video processing pipeline including an input coupled to the switch network output, wherein the switch network is configured to connect any of the video decoder outputs to any of the video processing pipeline inputs.

2. (Previously Presented) The apparatus of claim 1, further comprising an image size/location logic coupled to each video processing pipeline output, the image size/location logic configured to receive a signal indicating a designated size of a display window and which of the plurality of video sources includes video data for display in the display window, the image size/location logic further configured to determine a location in the display window and a size of a part of the display window for display for the video data for each of the plurality of video sources including video data for display.

3. (Previously Presented) The apparatus of claim 2, further comprising a plurality of scalers coupled to the plurality of video decoders and the plurality of video processing pipelines, wherein the plurality of scalers are each configured to scale the decoded video data from the plurality of video sources based on the determined size of the part of the display window.

4. (Previously Presented) The apparatus of claim 1, wherein the plurality of video processing pipelines are configured to process the decoded video data of the plurality of video sources received from the plurality of video decoders.

5. (Previously Presented) The apparatus of claim 4, wherein the apparatus comprises a greater number of video decoders than video processing pipelines and wherein the apparatus further comprises a display/control logic coupled to the plurality of video processing pipelines, the display/control logic configured to control a process order of the video data from the plurality of video sources.

6. (Previously Presented) The apparatus of claim 1, further comprising:

a memory device; and

a write multiplexer coupled to the memory device and the plurality of video processing pipelines, the write multiplexer configured to receive processed decoded video data from the plurality of video processing pipelines and store the processed decoded video data from the plurality of video sources into the memory device.

7. (Previously Presented) A method for displaying video data from a plurality of video sources on a display, the method comprising:

receiving video data from each of the plurality of video sources;

decoding, with a plurality of video decoders, at least a portion of the video data received from the plurality of video sources;

inputting the decoded portion of the video data into a plurality of video processing pipelines via a switch network; and

processing, by the plurality of video processing pipelines, the decoded portion of the video data.

8. (Previously Presented) The method of claim 7, wherein the number of video decoders is greater than the number of video processing pipelines.

9. (Previously Presented) The method of claim 7, further comprising storing the processed decoded portion of the video data into a portion of a video buffer that is not updating the display.

10. (Previously Presented) The method of claim 9, further comprising switching the portion of the video buffer that is not updating the display with a portion of the video buffer that is updating the display, upon determining that the plurality of video processing pipelines has completed processing the decoded portion of the video data.

11. (Previously Presented) The method of claim 7, wherein decoding, with the plurality of video decoders, the portion of video data comprises decoding, with the plurality of video decoders, a frame in the video data.

12. (Previously Presented) The method of claim 7, wherein decoding, with the plurality of video decoders, the portion of video data comprises decoding, with the plurality of video decoders, a field of a frame in the video data.

13. (Previously Presented) The method of claim 7, wherein decoding, with the plurality of video decoders, the portion of video data comprises decoding, with the plurality of video decoders, a scaled field of a frame in the video data.

14. (Previously Presented) A method for displaying video data from a plurality of video sources, comprising:

receiving the video data from the plurality of video sources at a first video decoder and a second video decoder;

decoding, via the first video decoder, a first frame of the video data from a first video source;

decoding, via the second video decoder, a second frame of the video data from a second video source;

inputting the first decoded frame into a first video processing pipeline via a non-blocking switch network;

inputting the second decoded frame into a second video processing pipeline via the non-blocking switch network;

processing, by the first video processing pipeline, the first decoded frame;

processing, by the second video processing pipeline, the second decoded frame;

transmitting the processed first decoded frame into a first portion of a video buffer for updating the display with the processed first decoded frame; and

storing the second processed decoded frame into a second portion of the video buffer that is not updating the display.

15. (Previously Presented) The method of claim 14, wherein processing, by first video processing pipeline, the decoded first frame comprises determining whether a first video source coupled to the first video processing pipeline is in a failed state.

16. (Previously Presented) The method of claim 15, wherein processing, by the first video processing pipeline, the first decoded frame comprises outputting a blacked out frame for the first video source upon determining that the first video source is in a failed state.

17. (Previously Presented) The method of claim 14, further comprising switching the configuration of the second portion of the video buffer that is not updating the display with the configuration of the first portion of the video buffer that is updating the display upon determining that the first and second video processing pipelines have completed processing the first and second decoded frames.

18. (Previously Presented) The method of claim 14, wherein performing the following for each of the plurality of video sources further comprises scaling the first and second decoded frames based on the image size and the number of video sources.

19. (Previously Presented) A system for displaying video data comprising:

a plurality of video sources, wherein each of the plurality of video sources is configured to transmit video data via one of a plurality of video channels; and

a video logic coupled to the plurality of video channels, the video logic comprising:

a plurality of video decoders, wherein each of the plurality of video decoders is configured to receive the video data from one of the plurality of video sources and to decode the video data;

a plurality of video processing pipelines; and

a switch network coupled to the plurality of video decoders and the plurality of video processing pipelines, the switch network configured to connect any of the outputs from the plurality of video decoders to any of the inputs of the plurality of video processing pipelines, wherein one of the plurality of video processing pipelines is configured to process the decoded video data from a portion of the plurality of video decoders.

20. (Previously Presented) The system of claim 19, wherein the video logic further comprises an image size/location logic coupled to the plurality of video processing pipelines, the image size/location logic configured to receive a control input for a size and a location of a window in the video display terminal and a designated number of video sources to display in the window, wherein the image size/location logic is further configured to determine a location in the window and a size of a part of the window for display for the video data for each of the designated video sources.

21. (Previously Presented) The system of claim 20, wherein the video logic further comprises a plurality of scalers coupled to the plurality of video decoders and the plurality of video processing pipelines, wherein each of the plurality of scalers is configured to scale the decoded video data from one of the video sources based on the size of the part of the window determined by the image size/location logic.

22. (Previously Presented) The system of claim 19, wherein the video logic comprises a greater number of video decoders than video processing pipelines and wherein the video logic further comprises a display/control logic coupled to the plurality of video processing pipelines, the display/control logic configured to control an order of processing of the decoded video data in the designated video sources by the number of video processing pipelines.

23. (Previously Presented) The system of claim 19, wherein the one of the plurality of video processing pipelines is configured to execute a video fail operation if one of the plurality of video decoders does not lock onto the video data from one of the plurality of video sources within a predetermined time.

24. (Previously Presented) The system of claim 23, wherein the video fail operation comprises an output of a blacked out frame overlaid with a descriptive text to indicate video failure for the one of the video sources.

25. (Previously Presented) The system of claim 23, wherein the video fail operation comprises an output of a previous image for the one of the plurality of video channels overlaid with a descriptive text to indicate video failure.

26. (Original) The system of claim 19, wherein the video data is analog video data.

27. (Previously Presented) The system of claim 19, wherein the video logic further comprises a write multiplexer and a video buffer coupled to the plurality of video processing pipelines, wherein the write multiplexer is configured to write the processed decoded video data from the plurality of video processing pipelines into the video buffer.

28. (Original) The system of claim 27, wherein the video logic further comprises a clock multiplier network, the clock multiplier network to control a rate of operation of the write multiplexer.

29. (Cancelled).